reading the floating gate transistor by placing a read voltage on a control gate and detecting the current conducted between a source region and a drain region in the substrate.

29. (New) The method of claim 28, wherein the insulator includes amorphous silicon carbide (a-SiC).

30. (New) The method of claim 28, wherein the method further includes erasing the floating gate by applying an erase voltage to the transistor which is less than 12V.

31. (New) The method of claim 28, wherein the method further includes refreshing the charge placed on the floating gate.

32. (New) The method of claim 31, wherein refreshing the charge placed on the floating gate includes refreshing the charge at regular time intervals of less than 40s.

33. (New) The method of claim 31, wherein refreshing the charge placed on the floating gate includes refreshing the charge at regular time intervals every few seconds.

34. (New) A method for operating a floating gate transistor, comprising:

storing data on a floating gate by providing a control voltage on a control line and a write voltage on a data line such that charge is carried from a substrate to the floating gate through an insulator, wherein a barrier energy betweein the insulator and the floating is less than 3.3 eV;

reading the data on the floating gate by placing a read voltage on the control line and detecting the current conducted through the transistor at the data line; and

erasing the floating gate by applying an erase voltage to the transistor which is less than 12V.

35. (New) The method of claim 34, wherein the insulator includes amorphous silicon carbide (a-SiC).

36. (New) The method of claim 34, wherein the method further includes refreshing the charge placed on the floating gate.

37. (New) The method of claim 32, wherein refreshing the charge placed on the floating gate includes refreshing the charge at regular time intervals of less than 40s.

38. (New) The method of claim 32, wherein refreshing the charge placed on the floating gate includes refreshing the charge at regular time intervals every few seconds.

39. (New) A method for programming a floating gate transistor, comprising:

applying a potential difference across a floating gate, gate oxide, silicon substrate junction sufficient to excite electrons to the floating gate, wherein the floating gate and a-SiC junction has a barrier energy of less than 3.3 eV.

40. (New) The method of claim 39, wherein applying a potential difference across a floating gate, gate oxide, silicon substrate junction includes applying a potential difference across a floating gate, amorphous silicon carbide (a-SiC), silicon substrate junction.

41. (New) The method of claim 39, wherein applying a potential difference across a floating gate, gate oxide, silicon substrate junction sufficient to excite electrons to the floating gate includes producing hot electron injection.

42. (New) The method of claim 39, wherein applying a potential difference across a floating gate, gate oxide, silicon substrate junction sufficient to excite electrons to the floating gate includes producing Fowler-Nordheim tunneling.